PATENT
Customer No. 22,852
Attorney Docket No. 4173.0438

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
Tetsuya KUROSAWA	)	Group Art Unit: 1734
	)	
Application No.: 10/665,206	)	Examiner: Osele, Mark A.
	)	
Filed: September 22, 2003	)	Confirmation No.: 5743
	)	
For: METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE AND MANUFACTURING APPARATUS OF SEMICONDUCTOR DEVICE	)	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97(d)

Pursuant to 37 C.F.R. §§ 1.56 and 1.97(d), Applicant brings to the attention of the Examiner the documents on the attached listing. This Information Disclosure Statement is being filed after a Final Action and is accompanied by a fee of $180.00 as specified under § 1.17(p) and a certification as specified under § 1.97(e).

The listed foreign patent document was first cited in an Office Action mailed August 21, 2007, from the Japanese Patent Office in a counterpart foreign application, and this Information Disclosure Statement is being filed within three months of the mailing date of that communication.

A copy of the foreign patent document and the Japanese Office Action are enclosed. An English language abstract of the patent document is also provided. Concise Statements of relevance of the non-English language documents are set forth below:

1. Summary of the Office Action from the Japanese Patent Office

The technique which grinds a wafer having grooves to produce the semiconductor elements having a thickness of 20 μm or more and 100 μm or less is commonly-known (for example, see JP-A Hei 4-297056 (KOKAI)).

2. Document (JP-4-297056)

Document discloses a method for manufacturing a semiconductor element. The manufacturing method includes forming grooves from a front surface of a semiconductor wafer, and grinding a back surface of the semiconductor wafer to produce semiconductor elements. Document discloses that thickness of the semiconductor elements can be set to about 200 μm, further 50 μm or less, according to the manufacturing method of the semiconductor element.

Applicant does not necessarily endorse the conclusions set forth in the Japanese Office Action.

Applicant respectfully requests that the Examiner consider the listed documents and indicate that they were considered by making appropriate notations on the attached form.

This submission does not represent that a search has been made or that no better art exists and does not constitute an admission that each or all of the listed

documents are material or constitute "prior art." If the Examiner applies any of the documents as prior art against any claims in the application and Applicant determines that the cited documents do not constitute "prior art" under United States law, Applicant reserves the right to present to the Office the relevant facts and law regarding the appropriate status of such documents.

Applicant further reserves the right to take appropriate action to establish the patentability of the disclosed invention over the listed documents, should one or more of the documents be applied against the claims of the present application.

If there is any fee due in connection with the filing of this Statement, please charge the fee to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: November 2, 2007

By: _____
Selah C. Park
Reg. No. 57,127